

A 2.5 inch, 33Mpixel, 60 fps CMOS Image Sensor for UHDTV Application

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Abstract

We have developed a 7840 x 4360 pixel, 60 fps CMOS image sensor fabricated in 0.18 μ m 1P4M process that is used for an Ultra High Definition Television (UHDTV) camera system. The sensor architecture is designed with a modular approach which allows it to be highly scalable up to >100Mpixel while still maintaining its high throughput and low noise performance. This 33Mpixel sensor is designed with 16 parallel readout modules with each module including 490 per column gain, 490 12-bit successive approximation A/D, SRAM block, SRAM timing control and LVDS output port. The sensor achieves an aggregate data rate of 24.6Gbit/s and power consumption of less than 3.7W.

I. Introduction

The demand for higher resolution and higher speed image sensor greater than 60fps for use in broadcast cameras and digital cinema cameras has been increasing. To meet these demands, we have developed a sensor architecture that is highly scalable and modular. This architecture enabled us to design a family of large format sensors that achieves high frame rate and low noise performance. The 33Mpixel sensor presented is developed for an experimental UHDTV camera system [1] and is the highest resolution sensor we have achieved to date. In this paper we will discuss our design techniques and present the use of a 2D power and ground mesh grid over the pixel array to distribute the pixel supply across the sensor without sacrificing valuable silicon area.

II. Architecture

Figure 1 shows the floor plan of the 33Mpixel sensor and the modular approach to the architecture. The design of the chip can be broken down to 6 main building blocks, the pixel array, row logic, timing control, analog bias and column readout module. The final assembled building blocks fits into a standard reticle and the image sensor was designed without using stitching technology.

The pixel array consists of 7840 x 4360 total pixels of which 7680 x 4320 makes up the core active area. Pixel pitch is 3.8 μ m and the pixel employs 3T technology. The pixel timing row logic is driven from one side of the pixel array and the timing control is duplicated on the top and bottom corners of the chip. Duplicating the timing control logic allows the top and bottom column readout modules to operate relatively independent of each other. The top and bottom timing controls share only the main clock, reset and external frame timing control.

The design of the column readout module uses the column parallel successive approximation architecture similar to [2][3][4]. To meet the frame rate requirement, our design uses one ADC per column at a layout pitch of twice the pixel size, 7.6 μ m. The column readout module consists of 490 per column gain, 490 12-bit successive approximation A/D, two 490 x 12-bit SRAM block, independent SRAM timing control and a 12-bit parallel LVDS output port. Each column readout module reads out 1/16 of a pixel row for the entire data path to the digital LVDS output port. Figure 3 shows a simplified drawing of each column's data path. The pixel output is amplified with a programmable gain amplifier and the output is directly sampled into the ADC. The reset noise and offset of the column gain amplifier are sampled onto the ADC sample hold capacitors and therefore subtracted during the ADC conversion. Row wise noise is suppressed by careful decoupling of any single-ended common bias voltage across the array. ADC

comparator offset is suppressed with per column ADC calibration. The 12-bit ADC output is stored in the SRAM block for readout. Figure 2 shows the row timing of the sensor readout. The readout of the pixel, followed by analog gain and ADC conversion is completed within $3.8\mu\text{s}$ to achieve the 60 fps requirement of the UHDTV camera system. The readout of the digital data is delayed to overlap with the following row's ADC conversion. LVDS I/O data output signaling is used to reduce noise injection into the substrate from the digital readout. Deep Nwell is also used to isolate all the high speed digital circuitry. Further precaution to reduce noise cross talk is made by completing the digital readout before the next pixel row's sampling and gain operation. This limitation sets the minimum output data rate for the SRAM and LVDS readout to 250 MHz. The modular design technique allows the high speed digital readout path of each module to be localized and helps avoid any long high speed routing of the data. Another advantage is that each module's SRAM data output timing is independent of each other. It is therefore possible to scale up a sensor's horizontal resolution while maintaining the same row timing by simply adding additional column readout modules. At maximum data rate, the sensor outputs the data at a burst rate of 4Gpix/s and has an aggregate data rate of 24.6Gbit/s.

For large format, high resolution high speed image sensors, pixel power supply distribution and routing becomes a difficult challenge. Care must be taken to avoid any shading or noise coupling due to routing of the power supplies. This sensor uses a 2 dimensional stacked power and ground mesh routed on top of the pixel array to distribute the power supply to the pixel. Figure 4 shows a simplified drawing of the 2D mesh power and ground supply grid concept. The pixel supply V_{pix} is routed through Metal3, and the return ground V_{gnd} is routed on Metal4 in a 2D mesh grid. Each pixel is connected to V_{pix} directly to the supply grid through vias. The pixel bias current V_{in} for each column is located at the top and bottom of the pixel array and its return current is connected to the V_{gnd} grid. Both calculated analysis and parasitic extracted simulation show that the 2D mesh grid significantly reduces the IR drop across the array. The 2D mesh grid does not consume valuable silicon area as compare to what would have been needed to route nearly 200mA of supply current during pixel readout across the 29.8mm array. This design technique is also highly scalable with increase pixel resolution and it creates additional decoupling capacitance between power and ground, which further reduces transient noise on V_{pix} during the pixel readout operation.

III. Results

A summary of the sensor specification and characteristics are shown in Table 3. Figure 5 shows a photo of the sensor in a custom 720-pin ceramic PGA and Figure 6 is an image taken with the experimental camera system showing the entire angle view and an enlarged center area. The sensor shows no visible pattern associated with the modular design approach.

Reference

- [1] T. Yamashita, et. al., "Experimental color video capturing equipment with three 33-megapixel CMOS image sensors," *IS&T/SPIE 21st Annual Symposium, Jan., 2009*.
- [2] I. Takayanagi, et. al., "A 1-1/4 Inch 8.3M pixel Digital Output CMOS APS for UDTV Application," *ISSCC Dig. Tech. Papers*, Paper 12.3, Feb., 2003
- [3] I. Takayanagi, et. al., "A 1.25-inch, 60 Frames/s, 8.3M-Pixel Digital-Output CMOS Image Sensor," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2305-2314, Nov., 2005.
- [4] A. Krymski, et. al., "A High Speed, 240 frames/s, 4.1-Mpixel CMOS Sensor," *IEEE Trans. Electron Devices*, vol. 50, pp. 130-135, Jan., 2003.

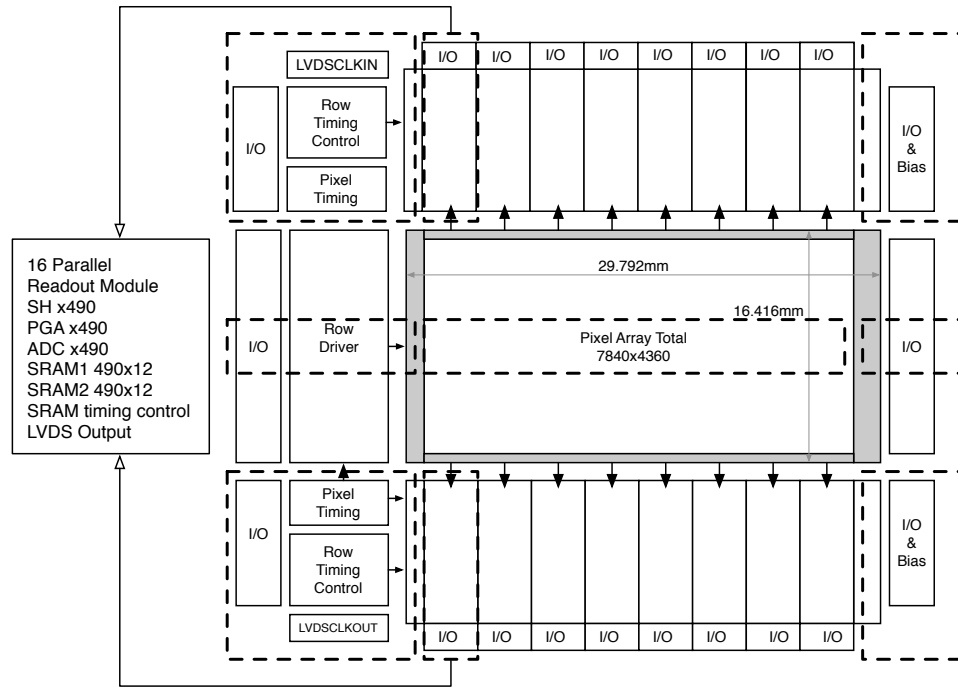


Figure 1 Modular Floor Plan

Parameter	Value
Technology	0.18um 1P 4M CMOS
Chip size	32.55mm x 25.55mm
Pixel size	3.8μm x 3.8μm
Number of total pixels	7840 (H) x 4360 (V)
Number of active pixels	7680 (H) x 4329 (V)
Frame Rate	60 fps
Column gain	x0.7, x1.0, x1.3, x2.0, x4.0
ADC	12 bit Successive Approximation
Column Readout Modules	16 @12 bit per port
Output Data Rate	250.56 MHz
Responsivity	11250 Bits / lux-s (output referred IR filter with 650 nm cutoff)
Conversion gain	0.21 LSB/electrons (output referred)
Pixel Noise floor in Hard Reset	50 e-
Full-well capacity	19000 e-
Power consumption	3.7W

Table 1. Specification and characteristics

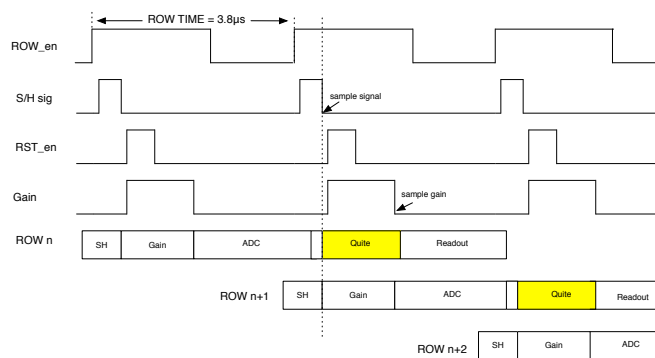


Figure 2 Row Timing Diagram

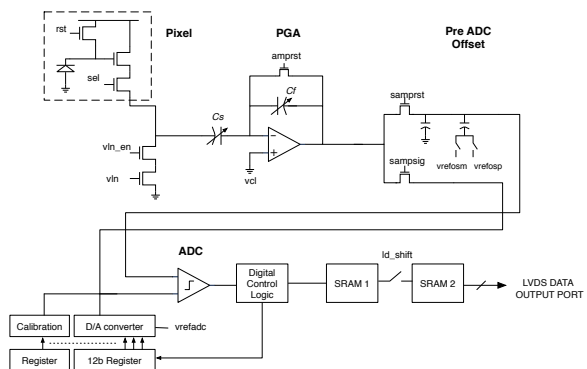


Figure 3 Column Circuit and Readout Path

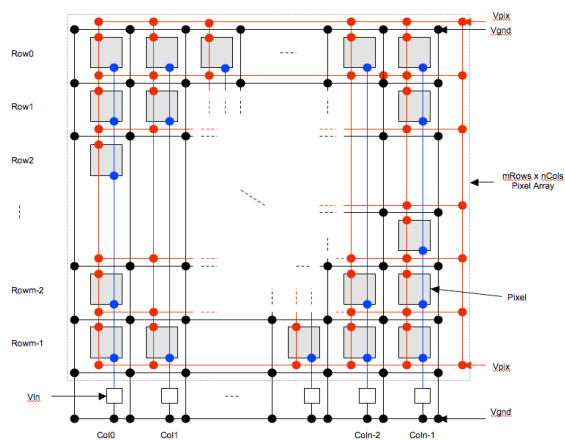


Figure 4. 2D Mesh Pixel Power and Ground Supply Routing

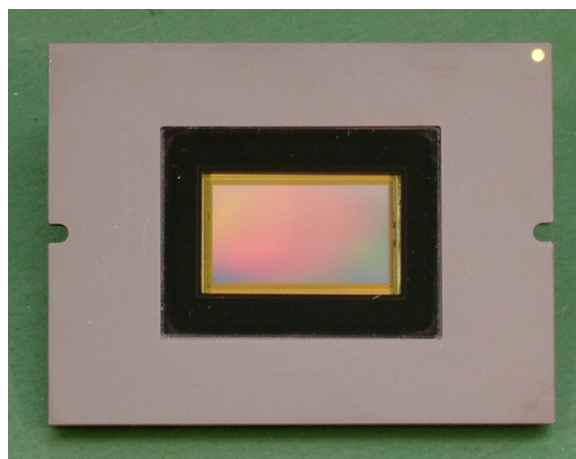


Figure 5. The sensor in a custom 720-pin ceramic PGA package



(1) Entire angle of view



(2) Center area (HD size)

Figure 6. Reproduced image